

## 40V N-Channel Enhancement Mode MOSFET

### Description

The AP280N04P/T uses advanced **SGT V** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 280A$

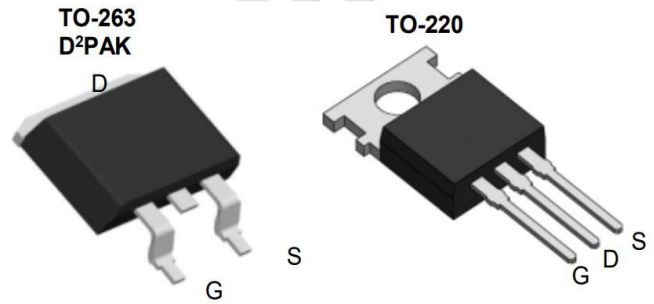
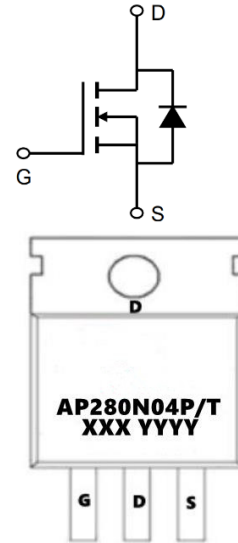
$R_{DS(ON)} < 1.5m\Omega$  @  $V_{GS}=10V$  (**Type: 1.2m $\Omega$** )

### Application

BMS

BLDC

UPS



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP280N04P	TO-220-3L	AP280N04P XXX YYYY	1000
AP280N04T	TO-263-3L	AP280N04T XXX YYYY	800

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_{D@TC=25^\circ C}$	Continuous Drain Current, $V_{GS} @ 10V$	280	A
$I_{D@TC=100^\circ C}$	Continuous Drain Current, $V_{GS} @ 10V$	200	A
$I_{DM}$	Pulsed Drain Current	1120	A
$E_{AS}$	Single Pulsed Avalanche Energy	818	mJ
$I_{AS}$	Avalanche Current	70	A
$PD@TC=25^\circ C$	Power Dissipation	230	W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	60	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.5	$^\circ C/W$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$



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### N-Channel Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

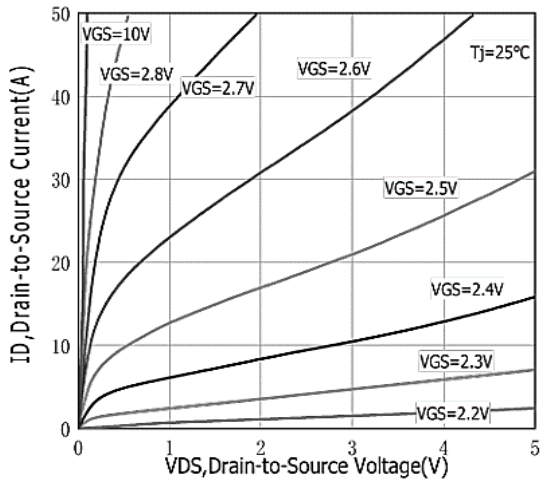
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	48	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	1.2	1.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	1.7	2.5	mΩ
Ciss	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1.0MHz	-	8300	-	pF
Coss	Output Capacitance		-	1510	-	pF
Crss	Reverse Transfer Capacitance		-	130	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =85A, V <sub>GS</sub> =10V	-	127	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	35	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	26	-	nC
td(on)	Turn-on Delay Time	V <sub>DD</sub> =20V, I <sub>D</sub> =85A, R <sub>G</sub> =1.6Ω, V <sub>GS</sub> =10V	-	22.5	-	ns
tr	Turn-on Rise Time		-	6.7	-	ns
td(off)	Turn-off Delay Time		-	80.3	-	ns
tf	Turn-off Fall Time		-	26.9	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	300	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	750	A
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>F</sub> =I <sub>S</sub> , dI/dt=100A/μs	-	100	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	163	-	nC

**Note :**

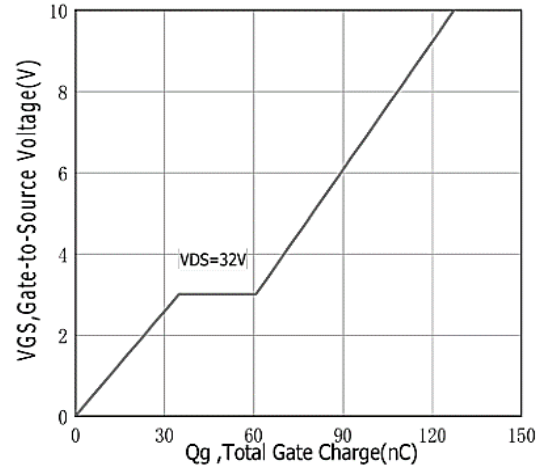
- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 20Z copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is VDD =32V,VGS =10V,L=0.1mH,IAS =70A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

**40V N-Channel Enhancement Mode MOSFET**

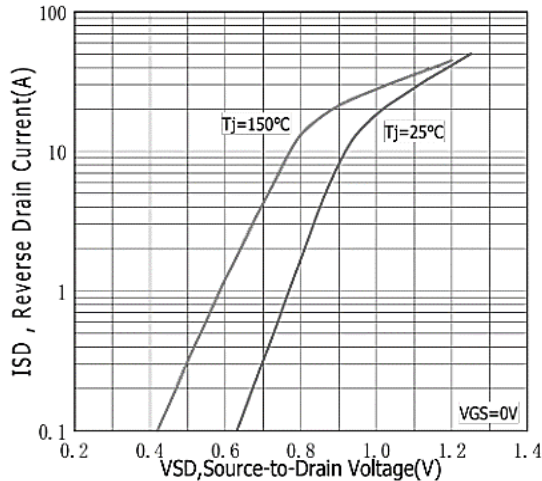
**Typical Characteristics**



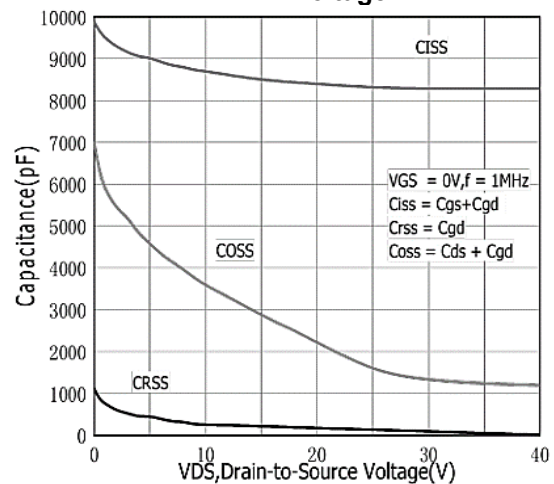
**Figure.1 Typical Output Characteristics**



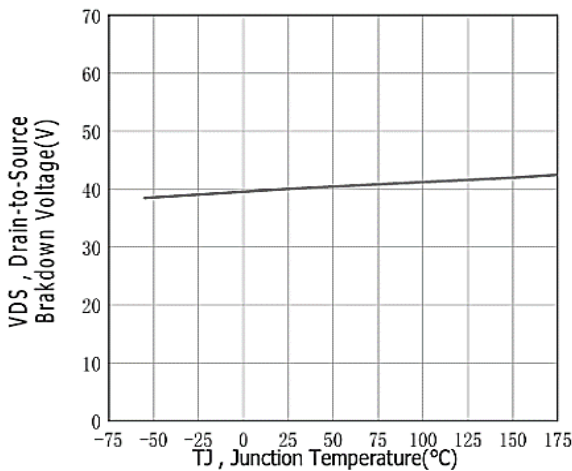
**Figure.2 Typical Gate Charge vs Gate to Source Voltage**



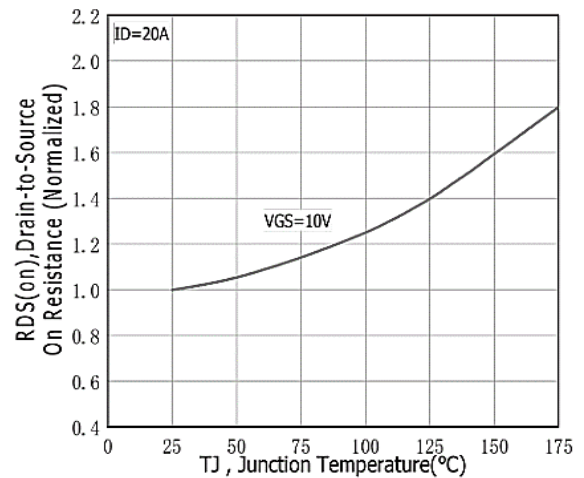
**Figure.3 Typical Body Diode Transfer Characteristics**



**Figure 4: Body Diode Characteristics**

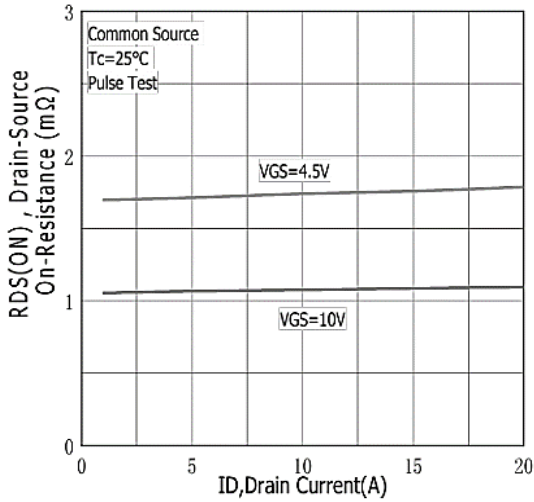


**Figure.5 Typical Breakdown Voltage vs Junction Temperature**

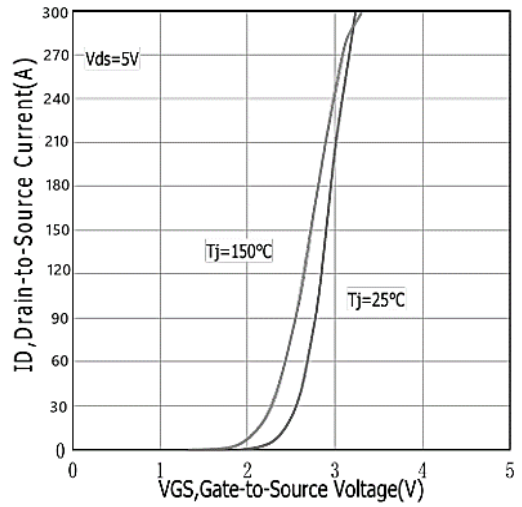


**Figure 6: Capacitance Characteristics**

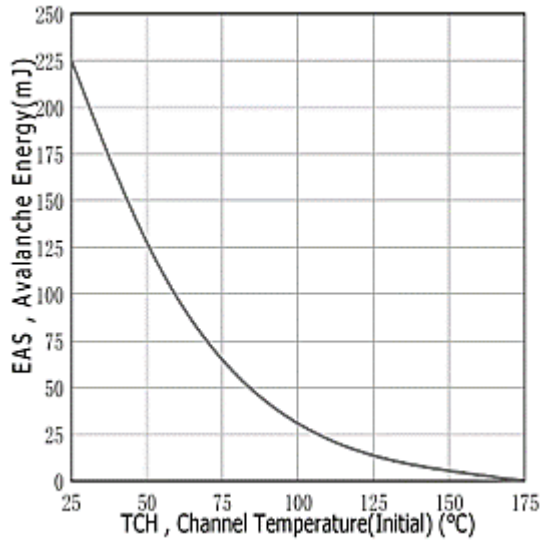
**40V N-Channel Enhancement Mode MOSFET**



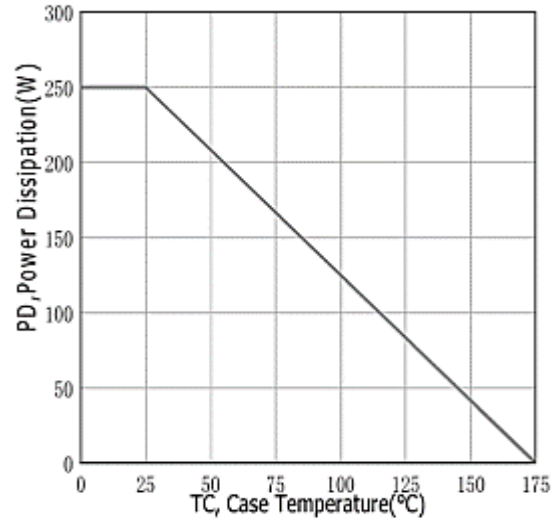
**Figure.7 Typical Drain to Source ON Resistance vs Drain Current**



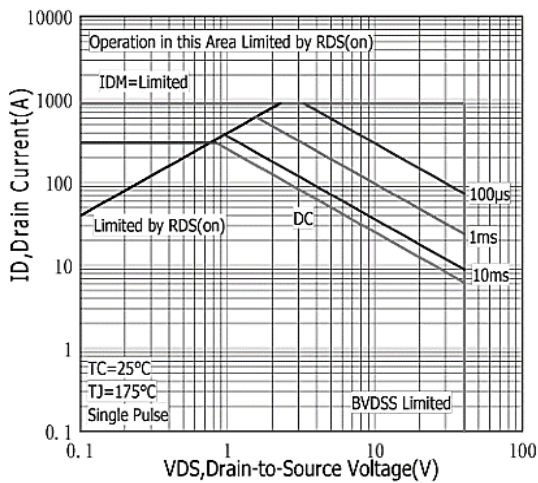
**Figure.10 Typical Transfer Characteristics**



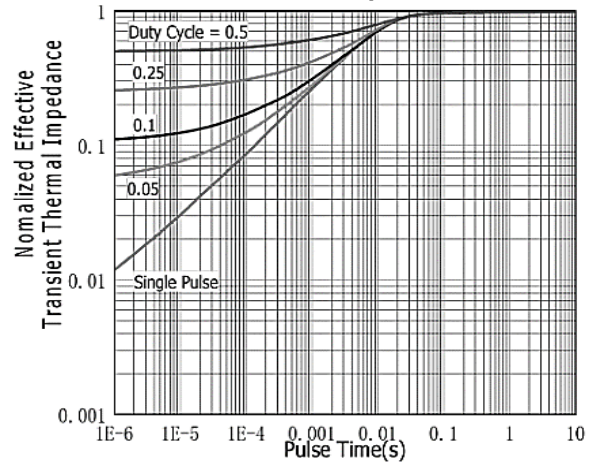
**Figure.9 Maximum EAS vs Channel Temperature**



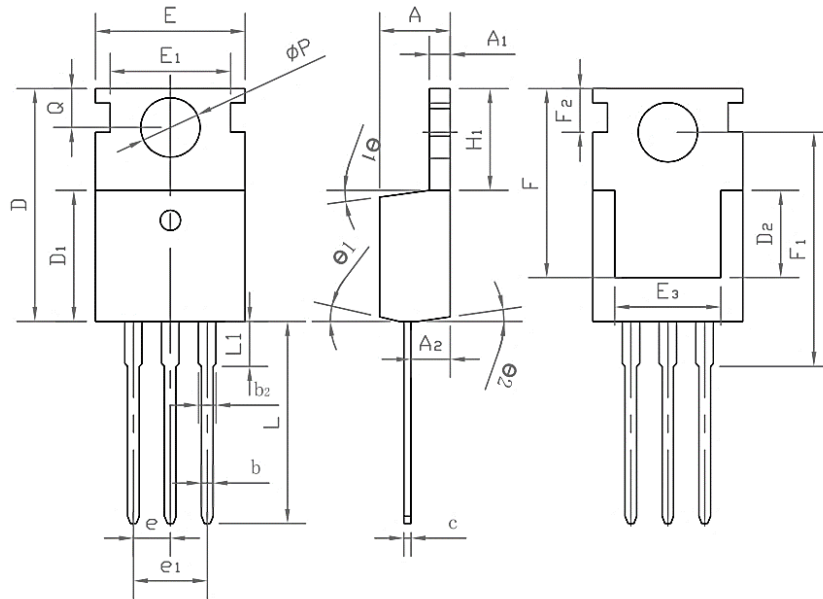
**Figure.12 Maximum Power Dissipation vs Case Temperature**



**Figure 11: Maximum Safe Operating Area**



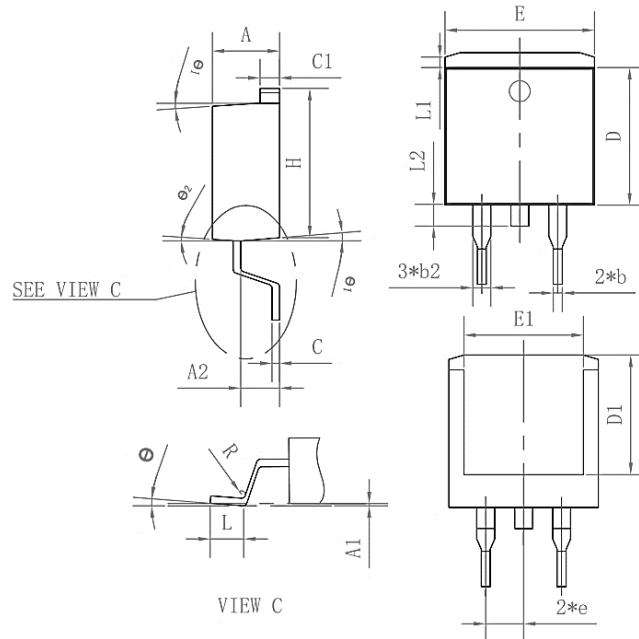
**Figure.12: Maximum Effective Transient Thermal Impedance, Junction-to-Cas**

**Package Mechanical Data-TO-220-3L-SLK**


Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e		0.37	
e1		0.10	
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
ϕp	3.45	3.60	3.75
Q	2.60	2.80	3.00
θ1	4°	7°	10°
θ2	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

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### Package Mechanical Data-TO-263-3L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.35	4.47	4.60
A1	0.09	0.10	0.11
A2	2.30	2.40	2.70
b	0.70	0.80	1.00
b2	1.25	1.36	1.50
C	0.45	0.50	0.65
C1	1.29	1.30	9.40
D	9.10	9.20	9.30
D1	7.90	8.00	8.10
E	9.85	10.00	10.20
E1	7.90	8.00	8.10
H	15.30	15.50	15.70
e	-	2.54	-
L	2.34	2.54	2.74
L1	1.00	1.10	1.20
L2	1.30	1.40	1.50
R	0.24	0.25	0.26
θ	0°	4°	8°
θ1	4°	7°	10°
θ2	0°	3°	6°